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09998848 - GAI: 2191

PTO/SB/08a (03-09)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		09998848
	Filing Date		2001-11-15
	First Named Inventor	Kenneth Y. Ogami	
	Art Unit	2191	
	Examiner Name	VO, TED T	
	Attorney Docket Number	CD01177	

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6460172	B1	2002-10-01	Insenser Farre et al.	Entire Document
	2	5399922	B1	1995-03-21	Kiani et al.	Entire Document
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9	5258760	B1	1993-11-02	Moody et al.	Entire Document
10	5563526	B1	1996-10-08	Hastings et al.	Entire Document
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21	4138671	B1	1997-02-06	Comer et al.	Entire Document
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NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1	Goodenough, F. "Analog Counterparts of FPGAS Ease System Design" Electronic Design, Penton Publishing, Cleveland, OH, US vol. 42, no. 21, 10/14/1994; 10 pages	<input type="checkbox"/>
	2	Harbaum, T. et al. "Design of a Flexible Coprocessor Unit" Proceedings of the Euromicro Conference, XX XX, Sept. 1999; 10 pages	<input type="checkbox"/>
	3	USPTO Application Number 09/924,734 (CD00169): "Programmable Microcontroller (PSoC) Architecture (Mixed Analog/Digital)"; Snyder et al., filed on 08/07/01; 28 pages	<input type="checkbox"/>
	4	USPTO Application Number 09/909,045 (CD00170): "Digital Configurable Macro Architecture," Warren Snyder, filed on 07/18/2001; 37 pages	<input type="checkbox"/>

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5	USPTO Application Number 09/909,109 (CD00172): "Configuring Digital Functions in a Digital Configurable Macro Architecture," Warren Snyder, filed on 07/18/2001; 38 pages	<input type="checkbox"/>
6	USPTO Application Number 09/909,047 (CD00173): "A Programmable Analog System Architecture," Monte Mar, filed on 07/18/01; 60 pages	<input type="checkbox"/>
7	USPTO Application Number 09/930,021 (CD00174): "Programmable Methodology and Architecture for a Programmable Analog System"; Mar et al., filed on 08/14/2001; 87 pages	<input type="checkbox"/>
8	USPTO Application Number 09/969,311 (CD00175): "Method for Synchronizing and Resetting Clock Signals Supplied to Multiple Programmable Analog Blocks," Bert Sullam, filed on 10/01/01; 57 pages	<input type="checkbox"/>
9	USPTO Application Number 09/875,599 (CD00180): "Method and Apparatus for Programming a Flash Memory," Warren Snyder, filed on 06/05/2001; 23 pages	<input type="checkbox"/>
10	USPTO Application Number 09/975,115 (CD00182): "In-System Chip Emulator Architecture," Snyder et al., filed on 10/10/2001; 38 pages	<input type="checkbox"/>
11	USPTO Application Number 09/953,423 (CD00187): "A Configurable Input/Output Interface for a Microcontroller," Warren Snyder, filed on 09/14/2001; 28 pages	<input type="checkbox"/>
12	USPTO Application Number 09/893,050 (CD00199): "Multiple Use of Microcontroller Pad," Kutz et al., filed on 06/26/2001; 21 pages	<input type="checkbox"/>
13	USPTO Application Number 09/929,891 (CD00226): "Programming Architecture for a Programmable Analog System," Mar et al., filed on 08/14/2001; 82 pages	<input type="checkbox"/>
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15	USPTO Non-Final Rejection for 09/994,601 (CD01170M) dated 11/14/2006; 15 pages	<input type="checkbox"/>

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	16	USPTO Final Rejection for 09/994,601 (CD01170M) dated 03/08/2000; 11 pages	<input type="checkbox"/>
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27	USPTO Application Number 09/972,003 (CD00176): "Test Architecture for Microcontroller Providing for a Serial Communication Interface," Warren Snyder, filed on 10/05/2001; 32 pages	<input type="checkbox"/>
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